We Claim:

1. A memory medium comprising program instructions for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, wherein the program instructions are executable to perform:

a) converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user;

b) configuring the programmable hardware element with the first hardware configuration program;

c) executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing; and

d) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program.

2. The memory medium of claim 1, wherein the program instructions are further executable to implement:

repeating a) – d) one or more times, wherein in each iteration of a) – d) the first portion of the program is a successively larger portion of the program.

3. The memory medium of claim 1, wherein the program instructions are further executable to implement:

repeating a) – d) a plurality of times;

wherein, in a first subset of iterations of a) – d) the first portion of the program is a successively larger portion of the program; and

wherein, in a second subset of iterations of a) – d) the first portion of the program is a successively smaller portion of the program.

4. The memory medium of claim 1, wherein the program instructions are further executable to implement:

after the program has been debugged,

converting the program into a second hardware configuration program which is deployable on the programmable hardware element to perform the function; and

configuring the programmable hardware element with the second hardware configuration program.

5. The memory medium of claim 1,

wherein said converting the first portion of the program into a first hardware configuration program comprises receiving user input indicating the first portion of the program.

6. The memory medium of claim 1, wherein the programmable hardware element is coupled to one or more hardware resources, and wherein said executing further comprises:

invoking the one or more hardware resources to perform the function.

7. The memory medium of claim 6, wherein the program is specified to access the one or more hardware resources, and wherein the program instructions are further executable to perform:

prior to said configuring the programmable hardware element with the first hardware configuration program,

analyzing the remaining portion of the program and the one or more hardware resources;

determining a test feed-through configuration based on said analyzing, wherein the test feed-through configuration is deployable on the programmable hardware element to provide for communication between the remaining portion of the program and the one or more hardware resources; and

including the test feed-through configuration in the first hardware configuration program;

wherein said configuring the programmable hardware element with the first hardware configuration program further comprises configuring the programmable hardware element with the test feed-through configuration; and

wherein said executing the remaining portion of the program further comprises the remaining portion of the program communicating with the one or more hardware resources through the programmable hardware element.

8. The memory medium of claim 7, wherein the program instructions are further executable to implement:

repeating a) – d) one or more times, wherein in each iteration of a) – d) the first portion of the program is a successively larger portion of the program.

9. The memory medium of claim 8, wherein in each iteration of a) – d), said determining a test feed-through configuration and said including the test feed-through configuration in the first hardware configuration program are performed only if the remaining portion of the program is specified to access the one or more hardware resources.

10. The memory medium of claim 8, wherein in each iteration of a) – d), said determining the test feed-through configuration comprises modifying the test feed-through configuration based on said analyzing the remaining portion of the program.

11. The memory medium of claim 7, wherein the program instructions are further executable to implement:

repeating a) – d) a plurality of times;

wherein, in a first subset of iterations of a) – d) the first portion of the program is a successively larger portion of the program; and

wherein, in a second subset of iterations of a) – d) the first portion of the program is a successively smaller portion of the program.

12. The memory medium of claim 7, wherein the program instructions are further executable to perform:

determining the one or more hardware resources.

13. The memory medium of claim 12, wherein said determining the one or more hardware resources comprises:

receiving user input indicating the one or more hardware resources.

14. The memory medium of claim 12, wherein said determining the one or more hardware resources comprises:

querying the one or more hardware resources.

15. The memory medium of claim 7, wherein said determining the test feed-through configuration comprises:

determining a plurality of pre-compiled hardware configuration program components; and

assembling the plurality of pre-compiled hardware configuration program components, thereby generating the test feed-through configuration.

16. The memory medium of claim 7, wherein said determining the test feed-through configuration comprises:

generating a test feed-through software program based on said analyzing; and

compiling the test feed-through software program, thereby generating the test feed-through configuration.

17. The memory medium of claim 16, wherein the program instructions are further executable to perform:

storing the test feed-through configuration on the computer system, wherein the stored test feed-through configuration is retrievable for use in other reconfigurable systems using the one or more hardware resources.

18. The memory medium of claim 7, wherein said determining the test feed-through configuration comprises:

determining a plurality of pre-compiled hardware configuration program components;

assembling the plurality of pre-compiled hardware configuration program components, thereby generating a first portion of the test feed-through configuration;

generating a test feed-through software program based on said analyzing;

compiling the test feed-through software program, thereby generating a second portion of the test feed-through configuration; and

combining the first portion of the test feed-through configuration and the second portion of the test feed-through configuration, thereby generating the test feed-through configuration.

19. The memory medium of claim 7, wherein at least a subset of the one or more hardware resources comprises one or more hardware cartridges.

20. The memory medium of claim 19, wherein at least one of the one or more hardware cartridges comprises an I/O cartridge.

21. The memory medium of claim 1, wherein the first portion of the program comprises a substantially debugged portion of the program.

22. The memory medium of claim 1, wherein the computer system executing the remaining portion of the program simulates execution of the remaining portion of the program on the programmable hardware element.

23. A memory medium comprising program instructions for debugging a program, wherein the program is usable to configure a reconfigurable system, wherein the program performs a function, wherein the reconfigurable system includes a programmable hardware element, wherein the program is intended for deployment on the programmable hardware element, wherein the program instructions are executable to perform:

a) receiving user input indicating a first portion of the program for deployment on the programmable hardware element, wherein a remaining portion of the program is to be debugged by a user;

b) converting the first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function;

c) configuring the programmable hardware element with the first hardware configuration program;

d) executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing; and

e) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program.

24. The memory medium of claim 23, wherein the program instructions are further executable to implement:

after the program has been debugged,

converting the program into a second hardware configuration program which is deployable on the programmable hardware element to perform the function; and

configuring the programmable hardware element with the second hardware configuration program;

25. The memory medium of claim 23, wherein the program instructions are further executable to implement:

repeating a) – e) one or more times, wherein in each iteration of a) – e) the first portion of the program is a successively larger portion of the program.

26. The memory medium of claim 23, wherein the program instructions are further executable to implement:

repeating a) – e) a plurality of times;

wherein, in a first subset of iterations of a) – e) the first portion of the program is a successively larger portion of the program; and

wherein, in a second subset of iterations of a) – e) the first portion of the program is a successively smaller portion of the program.

27. A memory medium comprising program instructions for debugging a program, wherein the program is usable to configure a reconfigurable system, wherein

the program performs a function, wherein the reconfigurable system includes a programmable hardware element, wherein the program is intended for deployment on the programmable hardware element, wherein the program instructions are executable to perform:

receiving user input indicating a first portion of the program for deployment on the programmable hardware element, wherein a first remaining portion of the program is to be debugged by a user;

converting the first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function;

configuring the programmable hardware element with the first hardware configuration program;

executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the first remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing;

receiving user input modifying the remaining portion of the program to debug the remaining portion of the program;

receiving user input indicating a second portion of the program for deployment on the programmable hardware element, wherein the second portion of the program comprises the first portion of the program and a debugged portion of the first remaining portion of the program, wherein a second remaining portion of the program is to be debugged by a user, wherein the second remaining portion comprises only a subset of the first remaining portion of the program;

converting the second portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function;

configuring the programmable hardware element with the first hardware configuration program;

executing the program, wherein said executing comprises:

the programmable hardware element executing the second portion of the program; and

the computer system executing the second remaining portion of the program.

28. A system for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, the system comprising:

a reconfigurable device, comprising:

a programmable hardware element; and

a computer system comprising a processor and a memory;

wherein the computer system is coupled to the reconfigurable device;

wherein the memory stores program instructions which are executable by the processor to:

a) convert a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user;

b) configure the programmable hardware element with the first hardware configuration program;

c) execute the program, wherein in executing the program:

the programmable hardware element executes the first portion of the program; and

the computer system executes the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing; and

d) receive user input modifying the remaining portion of the program to debug the remaining portion of the program.

29. The system of claim 28, wherein the program instructions are further executable to:

repeat a) – d) one or more times, wherein in each iteration of a) – d) the first portion of the program is a successively larger portion of the program.

30. The system of claim 28, wherein the program instructions are further executable to implement:

repeating a) – d) a plurality of times;

wherein, in a first subset of iterations of a) – d) the first portion of the program is a successively larger portion of the program; and

wherein, in a second subset of iterations of a) – d) the first portion of the program is a successively smaller portion of the program.

31. The system of claim 28, wherein the program instructions are further executable to:

after the program has been debugged,

convert the program into a second hardware configuration program which is deployable on the programmable hardware element to perform the function; and

configure the programmable hardware element with the second hardware configuration program.

32. A system for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, comprising:

means for a) converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user;

means for b) configuring the programmable hardware element with the first hardware configuration program;

means for c) executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing; and

means for d) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program.

33. The system of claim 32, further comprising:

means for repeating a) – d) one or more times, wherein in each iteration of a) – d) the first portion of the program is a successively larger portion of the program.

34. The system of claim 32, further comprising:

means for repeating a) – d) a plurality of times;

wherein, in a first subset of iterations of a) – d) the first portion of the program is a successively larger portion of the program; and

wherein, in a second subset of iterations of a) – d) the first portion of the program is a successively smaller portion of the program.

35. The system of claim 32, wherein the program instructions are further executable to implement:

after the program has been debugged,

means for converting the program into a second hardware configuration program which is deployable on the programmable hardware element to perform the function;

means for configuring the programmable hardware element with the second hardware configuration program.

36. A method for debugging a program, wherein the program is intended for deployment on a programmable hardware element to perform a function, the method comprising:

a) converting a first portion of the program into a first hardware configuration program which is deployable on the programmable hardware element to perform a corresponding first portion of the function, wherein a remaining portion of the program is to be debugged by a user;

b) configuring the programmable hardware element with the first hardware configuration program;

c) executing the program, wherein said executing comprises:

the programmable hardware element executing the first portion of the program; and

the computer system executing the remaining portion of the program;

wherein the remaining portion of the program is operable to be analyzed and debugged in response to said executing; and

d) receiving user input modifying the remaining portion of the program to debug the remaining portion of the program.

37. The method of claim 36, the method further comprising:

repeating a) – d) one or more times, wherein in each iteration of a) – d) the first portion of the program is a successively larger portion of the program.

38. The method of claim 36, further comprising:

repeating a) – d) a plurality of times;

wherein, in a first subset of iterations of a) – d) the first portion of the program is a successively larger portion of the program; and

wherein, in a second subset of iterations of a) – d) the first portion of the program is a successively smaller portion of the program.

39. The method of claim 36, the method further comprising:

after the program has been debugged,

converting the program into a second hardware configuration program which is deployable on the programmable hardware element to perform the function; and

configuring the programmable hardware element with the second hardware configuration program.